ABSTRACT OF THE DISCLOSURE

A thin film transistor array substrate for a liquid crystal display includes a substrate, and a gate line assembly formed on the substrate to receive gate signals. The gate line assembly has gate lines proceeding in the horizontal direction, and gate electrodes connected to the gate lines. A storage capacitor line assembly proceeds in the horizontal direction. A gate insulating layer is formed on the substrate while covering the gate lines and the storage capacitor line assembly. A semiconductor pattern is formed on the gate insulating layer over the gate electrodes. A data line assembly is formed on the gate insulating layer. The data line assembly has data lines crossing over the gate lines to define pixel regions, source electrodes connected to the data lines while being placed on the semiconductor pattern, and drain electrodes facing the source electrodes around the gate electrodes while being placed on the semiconductor pattern. A protective layer covers the data line assembly and the semiconductor pattern with contact holes. Pixel electrodes are formed on the protective layer at the respective pixel regions such that the pixel electrodes are connected to the drain electrodes through the contact holes. The gate lines or the pixel electrodes are provided with repair members, and the repair members are partially overlapped with the front gate lines or the pixel electrodes.